

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0037] with the following amended paragraph:

5 Please refer to Fig. 7 (also refer to Fig. 5 and 6). Fig. 7 is a diagram of the circuit of the control logic 62 according to the present invention. Due to the process of generating the control code simplified by the present invention, the control logic 62 only needs inverters 84 and AND gates 86. As mentioned above, when the input code 76 represents a
10 positive value, the sign code A3 is "0", the positive control code 78A being equal to the value code 82, all negative control bits X0 to X2 being "0". According to the control logic 62, the positive control bits Y0 to Y2 are generated by inverting AND operations of the value sign codes 82 A0 to A2 and the inverted sign code A3 respectively. When the input
15 code 76 represents a negative code, the sign code A3 is "1", the negative control bits are generated by the inverter of the value code 82, all positive control bits being "0". First, the bits A0 to A2 are separately converted and are then calculated with the sign code A3 for generating the negative control bits X0 to X2. When the sign code A3 is "1", the
20 control bits X0 to X2 are respectively equal to the inverted values of the bits A0 to A2 to define the relationship of Fig. 6. In Fig. 7, the control logic in the present invention only needs forty-four transistors (four inverters 84 including eight transistors, and six AND gates including thirty-six transistors). Compared to the prior art control logic 12
25 needing more than ninety transistors, the present invention saves a lot of transistors and reduces the layout size of the control logic, and further reduces the power waste and delays of the gates.

Please replace paragraph [0039] with the following amended paragraph:

30 Please refer to Fig. 8. Fig. 8 is a diagram of the converter in the present invention expanded to N bits. A converter 90 receives an N-bit

input code 106 and provides a corresponding output voltage V_o . There are N bits $A(N-1)$ to $A(0)$ in the input code 106, the bit $A(N-1)$ being the most significant bit. The converter 90 comprises a control logic 92 and an electrical module 94. The positive control bits $Y(0)$ to $[[Y(N-1)]]$ $Y(N-2)$ and the negative control bits $X(0)$ to $[[X(N-1)]]$ $X(N-2)$ are generated by the control logic 92 corresponding to the input code 106. The electrical module 94 comprises a positive electrical module 96A, a negative electrical module 96B, a negative current source 102 as an assistant electrical module, an OP amp 74, and a resistance R . The positive electrical module 96A comprises $N-1$ positive current sources 98, the positive current sources 98 providing currents $(2^0)I$, $(2^1)I$ to $(2^{(N-2)})I$ by ascending powers of two. The switches between the positive current sources 98 and the node $A3$ are controlled by the positive control bits $Y(0)$, $Y(1)$ to $Y(N-2)$. In other words, the switch corresponding to the positive current source providing $(2^n)I$ is controlled by the control bit $Y(n)$ (n is from 0 to $(N-2)$). The negative electrical module 96B comprises $N-1$ negative current sources 100. The switch corresponding to the negative current source providing $(2^n)I$ is controlled by the control bit $X(n)$ (n is from 0 to $(N-2)$). The switch 72 between the negative current source 102 of the assistant electrical module and the node $N3$ is controlled by the sign code $A(N-1)$ of the input code 106, $A(N-1)$ being the most significant bit of the input code 106. The total current flowing through the node $N3$ establishes an output voltage through the resistance R .

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